A²SI

Application Note
Advanced AS-Interface IC

1 Features

- Actuator-Sensor Interface (AS-i) is the simplest automation networking solution.
- AS-Interface is the ideal choice for networking sensors and actuators in factory automation and process control environments.
- A²SI is best seen as a digital replacement for traditional cable tree architectures.
- It is especially suitable for lower levels of plant automation where simple (often binary) field devices, such as switches, need to communicate in a stand-alone local area automation network controlled by PLC or PC.

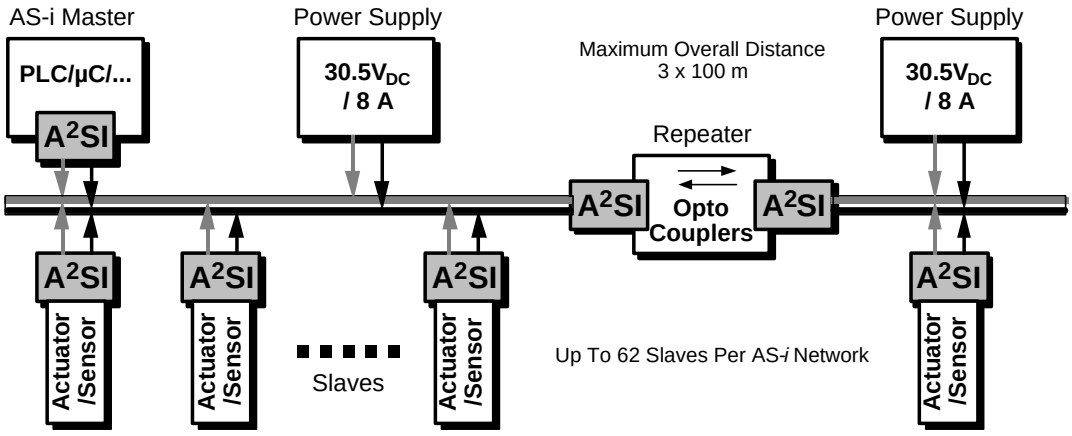
2 Description

AS-Interface is an open worldwide industry standard, IEC 62026-2 and EN 50295 (EU).

A²SI is the node in a cost-efficient, feature-rich ASI-based network carrying data and power over a single unshielded 2-wire cable that connects devices (slaves) to a host controller (master).

Complete Specification V2.11 compliant

3 A²SI Network Topology



4 Introduction

A²SI is a dedicated interface IC for AS-interface (Actuator Sensor Bus). Besides its special features as described in the A²SI Data Sheet, the IC is compliant to the Complete Specification AS-interface [1]. This application note refers to both documents and shall support practical issues concerning the application of the A²SI circuit. The following specific features are covered:

- Internal status register,
- EEPROM content and EEPROM programming techniques,
- A³SI operation modes (master, slave, and repeater mode),
- Status indication and security features, and
- Network set-up techniques (address reassignment)

Finally this document illustrates simple application circuits and deals with recommendations concerning necessary external components and PCB design issues.

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[1] Actuator Sensor Interface (AS-interface®) Complete Specification Version 2.11, 1.3.2000

[2] A²SI Data Sheet

[3] A²SI Revision C Release Notes

6 Scope

The application hints in this document should be understood as guidelines for designing with A²SI. No guarantee can be given for completeness or fully conformity to certain standards. A²SI has been designed to comply with IEC 62026-2 and EN 50295, but since A²SI is a component and not a complete system, other components in a system may influence or even jeopardize the performance of the whole system. Therefore, system conformity with standards is not the responsibility of ZMD but remains at the customer.

Recommendations are based on experience with various A²SI applications at this point in time and may be updated as more information becomes available. However, there is no guarantee that these recommendations will lead to a successful application in all cases.

It is recommended also to consult the A²SI Data Sheet for complete and detailed information about full features and properties of A²SI.

7 Configuration and Actuator Sensor Bus Operation

7.1. Important Registers

7.1.1. Status Register

Table 1 shows the IC's status register content. The use of status bits S0, S1 and S3 is compliant to the AS-Interface Complete Specification **[1]**. Status bit S2 is not used.

Table 1: A²SI Status Bits

Status Register Bit	Sx = 0	Sx = 1
S0	EEPROM write accessible	EEPROM access blocked (write in progress)
S1	FID == 0	FID == 1
S2	Static zero	N/A
S3	EEPROM content consistent	EEPROM contains corrupted data

7.1.2. Internal EEPROM

7.1.2.1. General Information

One special feature of the A²SI is its integrated EEPROM. This saves the otherwise necessary external EEPROMs (using conventional solutions) and thus contributes significantly to reductions in costs and the progressive miniaturization of slave modules. The non-volatile memory is divided into *user area* and a *firmware area*. The *user area* stores the address of a circuit configured as a slave, along with an ID_Code (ID code extension 1) assigned by the user. If the IC is operating in extended address mode, then most significant bit of this 4-bit data word is used to determine whether it is a so-called A-slave or B-slave (refer to section 7.2 Operation Modes for more detailed information).

The *firmware area* is used above all to select the operating mode (master, repeater, slave) and for storage of component-specific slave identification codes. Also, flags in this section enable or disable special IC features. By setting the *Program_Mode_Disable* flag in the EEPROM, the manufacturer of AS-i devices can protect the whole firmware area against accidental overwriting.

AS-i Complete Specification compliance note:

In order to ensure full compliance with the AS-i Complete Specification, the *Program_Mode_Disable* flag must be set in the final manufacturing and configuration process before an AS-i slave device is being delivered to field application users.

7.1.2.2. EEPROM Content

For security reasons the EEPROM is divided into several physically separated blocks. However, the user will not notice the internal organization since the EEPROM forms a single memory in terms of address organization. Table 2 shows the meaning of the sixteen 4-bit wide words.

Table 2: EEPROM Content

A²SI Internal EEPROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
0	0	A0	Slave Address Low Nibble
0	1	A1	
0	2	A2	
0	3	A3	
1	0	A4	Slave Address High Nibble
1	1 .. 3	(not usable)	Not relevant to A²SI functions
2	0	ID1_Bit0	ID_Code_Extension_1
2	1	ID1_Bit1	
2	2	ID1_Bit2	
2	3	ID1_Bit3	
3 .. 7	0 ..3	Logical not implemented - do not access	
8	0	ID_Bit0	ID_Code
8	1	ID_Bit1	
8	2	ID_Bit2	
8	3	ID_Bit3	
9	0	ID2_Bit0	ID_Code_Extension_2
9	1	ID2_Bit1	
9	2	ID2_Bit2	
9	3	ID2_Bit3	
A	0	IO_Bit0	IO_Configuration
A	1	IO_Bit1	
A	2	IO_Bit2	
A	3	IO_Bit3	
B	0	Multiplex	Configuration Flags
B	1	Reserved	
B	2	Reserved	
B	3	Watchdog_Active	
C	0	Master_Mode	Configuration Flags
C	1	Program_Mode_Disable	
C	2	Repeater_Mode	
C	3	Invert_Data_In	
D	0 .. 3	Logical not implemented - do not access	
E	0 .. 3	Analogue circuitry trim information Accessible by ZMD only	
F	0 .. 3		

User Area *Firmware Area*

7.1.2.3. EEPROM Write Access

A write access to the internal EEPROM is only possible if the A²SI IC is configured in Slave-Mode (refer to section 7.2). The EEPROM may then be programmed in two ways:

1. **Network component set-up: Transmission of the AS-i master calls *Address_Assignment* (ADRA) or *Write_Extended_ID_Code1* (WID1).**

For a functional description of the AS-i master calls, please refer to the AS-i Complete Specification [1]. Both calls are only available at slave address 0x0. By the definition of the master calls it is clear which EEPROM locations must be addressed even if no specific selection is made. The Address_Assignment will effect EEPROM address 0x0 and 0x1. The Write_Extended_ID_Code1 accesses EEPROM address 0x2.

These two commands are intended to be used when a slave is installed in the (sometimes rough) environment of the final application. Since an interruption of the programming process may corrupt the data stored at the EEPROM locations 0x0 to 0x2, the EEPROM write access is additionally monitored by a security flag.The security flag is non-volatile and will be set before the actual EEPROM content is modified. It will be reset when the data was successfully programmed.

The security flag is automatically read out after any reset (power-on-reset, external reset, reception of Reset_Slave or Broadcast_Reset calls) and copied to the IC status register bit S3. If the status bit is set the EEPROM content is considered to be corrupt. In order to reach a defined state after the initialization of the A²SI the slave address is then automatically set to 0x0. It is recommended that the master control procedure considers this while processing the network initialization procedure.

Important: If more than one slave needs to be reprogrammed within a running system, it is recommended to change the slave address or the ID-Code-Extension1 in one slave only at a time. After one slave has been reprogrammed successfully (indicated by the IC status word), the next slave can be reprogrammed.

2. **Invoking *Program Mode*: Transmission of *Write_Parameter* (WPAR) Calls.**

The *program mode* is intended to be used during production set-up of an AS-i slave component at the manufacturer's site. It can be entered only if slave address was set to 0x0. In the case that the slave address equals zero, the reception of the *Enter_Program_Mode* (PRGM) call sets the *Program_Mode* Flag within the A²SI. It should be noted that no response is generated to the *Enter_Program_Mode* call (refer to AS-i Complete Specification [1]).

If the *Program_Mode* flag is set, Write_Parameter (WPAR) and Data_Exchange (DEXG) calls have other meanings. The address bits A3...A0 of the master telegrams are then used to address one of the sixteen memory locations of the EEPROM (Table 2). Address bit A4 is don't care. The information bits I3...I0 (normally used for output data) carry the data which shall be stored or is read from the EEPROM. The Write Parameter initiates a write access. The Data_Exchange is used to read out a specific EEPROM word.

Important: In *Program_Mode* the A²SI will generally accept master calls of any slave address regardless of the value of its own address register.

However, any attempt to access one of the not available EEPROM address locations (0x3...0x7, 0xD) through a Write_Parameter (WPAR) or Data_Exchange (DEXG) command or an attempt to reprogram the trim registers (0xE, 0xF) will RESET the circuit.

Any *Write_Parameter* (WPAR) call initializes an autonomous write process within the IC. The status of the write process can be monitored by evaluating the status register of the IC. If bit S0 is set (logical '1') the write process is not finished yet and the programming data is still volatile. If bit S3 is set, the write procedure did not successfully complete either because the write cycle was interrupted or due to an internal error. In order to program the data correctly the write request should be repeated. The status register can be read using the AS-i Master call Read_Status.

7.1.2.4. Recommended EEPROM Access Procedures in Program Mode

As outlined above, the content of the EEPROM can be set-up in *program mode* using master call *Write_Parameter* (WPAR) for write access and *Data_Exchange* (DEXG) for read access for verifying programmed data. As read and write access can not be performed within a single AS-i cycle (master call + slave response), read and write procedures must apply to several rules:

Write Access:

In general, the slave status shall be checked after the master has issued a call that writes into the EEPROM. As long as the slave status indicates that the write process is still going on (S0 = 1, S3 = 0), no further EEPROM accesses should be requested (refer to 7.1.2.1 for AS-i Complete Specification compliance).

An EEPROM programming procedure should be created in consideration of the following steps:

1. Set slave address to zero (if not yet done) by using *Delete_Address* (DELA) call.

2. Enter the A²SI program mode by transmitting *Enter_Program_Mode* (PRGM) call.

3. Check the IC's status by using the *Read_Status* (RDST) call (this is recommended prior to attempting any write access to the EERPOM). If status bit S0 = 1, wait at least 128 ms and repeat this step.

4. Perform the write access by transmitting a *Write_Parameter* (WPAR) call. As already mentioned – compared with normal operation mode, WPAR works differently in *Program_Mode* (refer to section 7.1.2.3 and A²SI Data Sheet).

5. Check the IC's status again (*Read_Status* (RDST) call). If S0 was reset to '0', write cycle finished successfully and next EEPROM location may be accessed.

Read Access:

A *Read_Status* (RDST) call must be performed prior to reading a certain EEPROM address. As the RDST call will reset the EEPROM Read_Pointer, it is a mandatory part of the read procedure. Therefore, it must be applied, also if the slave status information is not intended to be retrieved at that moment.

Afterwards, the EEPROM should be read consecutively using the *Data_Exchange* (DEXG) call until the slave responds. The first DEXG call will only initiate the EEPROM read process for the selected EEPROM address. It will not generate a slave response! Subsequent DEXG calls will result in a response if the read process finished successfully.

One should consider that the returned value always relates to the address given in the first DEXG call regardless of a possibly different address in a subsequent call! In order to select a new address location after a completed read access, a *Read_Status* (RDST) call has to be sent again.

In principle, the EEPROM address shall be kept constant at consecutive *Data_Exchange* (DEXG) calls.

An EEPROM verification procedure should be created in consideration of the following steps:

1. Set slave address to zero (if not yet done) by using *Delete_Address* (DELA) call.

2. Enter A²SI™ Program_Mode by transmitting Enter_Program_Mode (PRGM) call.

3. Make sure that no write EEPROM access is being performed (check the IC's status) and reset EEPROM Read_Pointer using Read_Status call. If S0 = 1, wait a certain time (128 ms is recommended) and repeat this step.

4. Submit Data_Exchange (DEXG) calls until a response is received. The first DEXG will never be answered. Consider also the chance of transmission errors.

5. Continue reading other EEPROM addresses by starting at step (3) again.

7.2. Operation Modes

7.2.1. Overview

Basically, A²SI can operate in three modes. These are ***slave mode***, ***master mode***, and ***repeater mode***. After a reset, the circuit enters one of these modes depending on the non-volatile flags *Master_Mode_Bit* and *Repeater_Mode_Bit* (refer to section 7.1.2.2), see Table 3 below.

Table 3: A²SI Operation Modes

Mode	Master_Mode_Bit	Repeater_Mode_Bit	Remarks
Slave Mode	0	0	Program mode possible
Master Mode	1	0	Program mode impossible
Repeater Mode	1	1	Program mode impossible
Reserved	0	1	Reserved for future enhancements

ZMD delivers A²SI pre-programmed devices in two configurations:

- *Slave Mode:* By default A²SI ICs are delivered in slave mode. In this case, the entire EEPROM is cleared (all bits set to zero). Slave address is equal to zero and A²SI is operating in standard address mode (refer to 7.2). By entering program mode (refer to chapter 7.1.2.3), initial settings can be changed. An IC in slave mode can be configured to any other operational mode by using the program mode.

- *Master Mode:* Bit 0 (*Master_Mode_Bit*) at EEPROM address 0xC set to '1' selects master operation mode of the IC. The remaining memory space is cleared (all bits set to zero). In Master Mode, it is impossible to enter the program mode of the A²SI. Once the IC is set to Master Mode, the configuration cannot be changed again. Master Mode pre-programmed ICs are marked with a yellow colored dot.

  Check the A²SI Data Sheet or contact ZMD for detailed ordering information.

7.1.1 Regular Slave Operation

The AS-i Complete Specification **[1]** defines a new extended address mode which permits a maximum of 62 slaves to be operated on a single network, - an enhancement compared to the previous maximum of 31

slaves. Since the basic format of a telegram was not changed, slaves using old and new addressing standard can still work together in one system. However, it should be noted that *Standard Slaves* (slaves which use the old addressing standard) will consume two addresses of the address space which otherwise could be assigned to two slave addresses in extended mode.

To accommodate this enhancement, additional addresses were not simply counted up from 32 to 61, but two new types of slaves (A-type, B-type) were defined (**Figure 1).** A standard slave will be abbreviated with S-slave. A- and B-type slaves share the same 5-bit standard address but can be separated through *Information Bit* I3 of the Master telegram which acts as the select bit (see also AS-i Complete Specification **[1]**). **Figure 1** demonstrates the meaning of I3 changes in extended address mode. I3 cannot be used to transfer data from the master to the slave, thus the data word can only be 3 bits wide in this direction. However, data transfers from a slave to the master remain 4 bit wide.

Configuration information that defines whether a slave is in extended address mode or not depends on the value of the non-volatile ID-Code register. The AS-i Complete Specification [1] reserves the value 0xA as the ID-Code for slaves in extended address mode. Any other value of the ID-Code register sets the A²SI to standard address mode operation.

Configuration of an A- or B-Slave is done by bit 3 of *ID_Code_Extension_1* register. (user region of the EEPROM, refer to Table 2). If a slave is in extended address mode, the value of this bit is compared to the SEL bit (I3 bit) of the master call. The call is accepted if they match and address register of the slave equals the 5 address bits in the master telegram. It should be noted that bit I3 of a master telegram may represent the

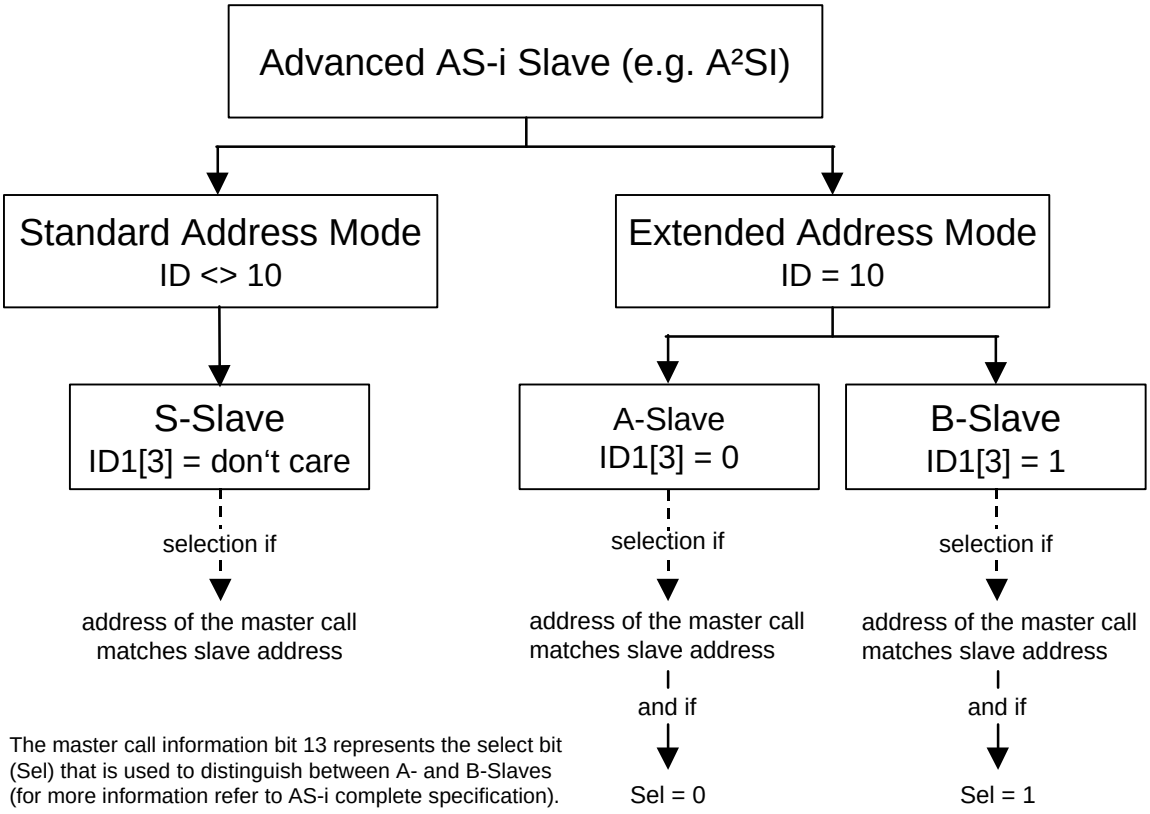


Figure 1: Slave Addressing Modes

bit (SEL) or the inverted select bit (~SEL) depending on type of call.

There are two exceptions to A-Slave/B-Slave select mechanism:

- It is not used if a slave was programmed to address zero. Slave address 0x0 shall be used for configuration purposes only. Therefore, there is no distinction between standard and extended address mode slaves. Settings of the registers *ID_Code* and *ID_Code_Extension_1* have no impact on slave address 0x0.

- Broadcast calls address all slaves in the network at the same time, no matter whether it is an A-Slave, a B-Slave or an S-Slave.

Bit I3 of a master telegram cannot be used for data communication in Extended Address Mode. Instead, it represents the A-Slave/B-Slave selector (SEL). Depending on the particular master call, bit I3 is equal to SEL or to ~SEL **[1]**.

It is not possible to mix the two addressing modes (*Standard Mode/Extended Address Mode*) on a single slave address (e.g. Standard Slave + B-Slave). Both addressing modes differ in the meaning of the I3 bit. The consequence would be that during DEXCH and WPAR transfers, a situation in which both slaves respond might occur.

7.2.3. The Special Behavior of Slaves with Address = 0

A slave programmed to address 0x0 behaves like an S-slave, regardless of the settings of *ID_Code* and *ID_Code_Extension1* registers.

7.2.4. Recommended Procedure to Change a Slave Address

If the address of a slave shall be reassigned, the user has to make sure that none of following two scenarios can occur:

- The new slave address is identical to the address of another *Standard Slave* in the network.

- The new slave type (A-type, B-type) is identical to another slave's type and both operate at the same slave address (extended address mode only).

Both scenarios will seriously jeopardize the network. There is no way out of such a miss-configuration except through local reprogramming of the slaves.

It is important to know that the A²SI will respond to modified addresses or slave types immediately after an appropriate master call (*Address_Assginment, Write_Var_ID_Code*) was received. Although an EEPROM write access will take about 512 ms for an *Address_Assignment* and 384 ms for a *Write_Var_ID_Code* command, the data affects the behaviour of the circuit immediately. The data is first stored in a volatile *Shadow Registers*, which directly control the behavior of the circuit.

Because of above-mentioned reasons, the following sequence of master calls should always be transmitted when slave addresses are going to be changed:

- ***Reset_Slave* (RES) Call.** A slave reset is especially recommended, if the communication watchdog is activated, otherwise a watchdog-reset (refer to chapter 7.2.6.2) could accidentally interrupt an EEPROM write access. A slave reset deactivates the watchdog function temporarily until the first Write_Parameter call has been received. This is because the watchdog is coupled to the status of *Data_Exchange_Disable* flag (Table 2). This flag is set during the initialization procedure of the A²SI and turns the watchdog off. The first Write_Parameter call resets the *Data_Exchange_Disable* flag and enables the watchdog.

- ***Delete_Address* (DELA) Call**. Sets slave address to zero.

- ***Write_Var_ID_Code* (WID1) Call**. A modification of *ID_Code_Extension1* (A-/B-slave selection by ID1_Bit3) must be done prior to any assignment of a new slave address to avoid the second failure

scenario described above. This requirement is only relevant for slaves that are intended to work in extended address mode.

- ***Read_Status*** **(RDST)**. Checks status of EEPROM write process. Repeat this command until S0 = 0 and S3 = 0. Only then, the previous EEPROM write process was successfully completed only as soon as both conditions apply.
- ***Address_Assignment*** **(ADRA)**. Assigns a new slave address. Note that a new slave address becomes active immediately after a call was received. All subsequent master calls must use this new address and shall not address 0x0.
- ***Read_Status*** **(RDST)**. Checks status of EEPROM write process. Repeat this command until S0 = 0 and S3 = 0. Only then, the new assigned address has been successfully written into the EEPROM.

7.2.5. EEPROM Data Integrity Check

After any reset (refer to section 7.2.6), the A²SI checks the integrity of the data in the user region of the EEPROM. If a preceding write access to the EEPROM did not finish successfully (e.g. because the system was powered down or the slave was reset before the write cycle ended), the IC will detect this immediately after power-on or any other reset. If the integrity check fails, the IC will set status bit S3 to '1' and clear the volatile address register so that the slave will respond to address 0x0 after initialization. While initializing a network, the master software should therefore start a relevant recovering procedure for slaves without proper EEPROM content.

Setting (volatile) slave address register to 0x0 can be considered as putting the IC into a defined state. In this state, it does not matter what the content of the slave address and *ID_Code_Extension1* registers in the EEPROM are, because both are possibly corrupted.

This functionality is only available for the user region of the EEPROM. It assumes that the firmware configuration of the A²SI is made under "safe" conditions at the site of the AS-i component manufacturer.

A write access to any of the EEPROM addresses is followed by a so-called read-back procedure. The read-back procedure checks the data that was actually stored in the EEPROM against data of the volatile shadow register. If there is a difference, status bit S3 will be set and the failure can be detected by a *Read_Status* call. A real read-back error indicates a severe error of the IC's hardware. If there is no evidence of a possible violation of operating conditions or any other procedures that may have resulted in the setting of the S3 bit, it is recommended to remove such a device from the system.

7.2.6. IC Reset

7.2.6.1. Operator Introduced Reset

Different events may lead to a reset of the A²SI. Following possibilities can be controlled by an operator directly:

- Power-On Reset.
- External Reset; pulling DSR pin low (logical 0) for more than 44µs triggers an unconditional reset. The IC resumes to its initialization procedure only after DSR was released to high-impedance state or pulled to a logical high level. While the IC is held in an idle state (DSR is pulled low), the LED pin is observed by special internal circuits. A certain logical sequence of an externally generated signal applied to LED pin could force the IC to enter a device test mode. The test mode is reserved for ZMD's production test requirements.
- Reset by Master Call; this reset is available in slave mode only. It can be triggered by sending a *Slave-Reset* (RES) or *Broadcast-Reset* (BR01) master call.

Power-on reset and an external reset are possible independent of operational mode of the A²SI (master, slave, or repeater mode).

7.2.6.2. Watchdog Reset

A Watchdog Reset can only occur in slave mode of the A²SI. Once the communication watchdog was activated (*Watchdog_active_Flag* set and *Data_Exchange_Disable_Flag* reset), it will trigger an unconditional reset as soon as it detects a data communication pause for more than 40 ms. It should be noted that only the reception of a *Write_Parameter* or a *Data_Exchange* call can reset the watchdog. Any other communication between master and slave is not monitored by the watchdog and may therfore cause a watchdog reset too, if the 40 ms time frame is exceeded.

7.2.6.3. Automatic Failure Status Reset

The A²SI incorporates counter-measurements against electromagnetic interference to further support the significant security standards of AS-i. In a rough industrial environment, the IC may enter a forbidden logical state caused by a strong electromagnetic pulse. Such forbidden states cannot be invoked through any normal operation but are detected by an independent logic that, eventually, leads the circuit back to a defined state. Once the state machine of the IC has entered a forbidden state, it is very likely that any of the other volatile IC registers may have become disrupted too. To account for this possibility, the A²SI performs an unconditioned reset immediately after such failure status was detected.

As mentioned in chapter 7.1.2, the A²SI will also be forced into a reset if any of the logically not implemented EERPOM addresses is being accessed (refer to Table 2).

7.2.6.4. Reset and Initialization Procedure

In any of the above mentioned reset events, the IC will set outputs to a high-impedance state, set the *Data_Exchange_Disable_Flag* to '1', and clear all remaining volatile flags and registers. It will then execute an initialization procedure that copies the content of the EEPROM to volatile (shadow) registers and checks the integrity of the EEPROM user data (refer to section 7.2.5).

To avoid an accidental test mode invocation, the PCB designer should pay attention to the maximum parasitic capacitance at the LED pin. In order to ensure proper functionality of the IC, the limit specified in A²SI Data Sheet shall not be exceeded, especially if LED pin is intended to be left open. An additional pull-up resistor to U_{OUT} may help if PCB parasitic capacitance exceeds the maximum allowed load at LED pin.

7.2.6.5. Over-Heating Shutdown

The chip temperature of the A²SI is continuously supervised. If it exceeds the maximum allowable value (e.g. caused by an overload), the circuit will automatically shut down. In this case, the outputs are switched to high-impedance state and the circuit enters an idle state. The idle state is left only after the next power cycle (a power-on reset requires a complete removal of the supply voltage).

7.2.7. AS-i Channel Selection

An A²SI circuit operating in slave mode has two AS-i input channels. The first one is the normal channel which can be connected to a standard AS-i cable (ASIP pin and ASIN pin). The second channel, the so-called *Infrared Addressing Channel*, is dedicated for simplified configuration of AS-i slaves in the final filed application.

The receiving path of the IR-channel is supported by a special photo-diode input (IRD) while the output transmitter utilizes the status indicator LED to send response telegrams.

After reset, the A²SI scans both channels continuously in sequence for about 500 µs per channel. If the A²SI recognizes a valid AS-i telegram at one of the inputs, it will lock the particular channel as for communication until next IC reset occurs. For more information about the IR-channel operation refer to section **7.4**.

To ensure that the IC has locked to the appropriate input channel, a couple of dummy calls should be send by the master or programming device, before "serious" communication is started.

7.3. Status Indicator LED

The LED output has two functions. It operates as status indicator output, if the AS-i line input channel is selected and the IC works in Slave Mode. Otherwise, if either the infrared input channel is selected, or if the IC works in Master Mode, the LED output maintains the output path of IR-channel.

The status indicator function was implemented according the definitions in the AS-i Complete specification **[1]**. **Figure 2** shows the LED output function by means of a schematic block diagram.

Operational mode of the LED depends on following information:

- *master_bit*: This flag is set in both Master Mode and repeater mode. It corresponds to master flag information stored in the EEPROM (address 0xC, bit 0).

- *irlock_bit*: This flag is set in Slave Mode if the IC has detected valid AS-i telegrams at the infrared addressing channel input (IRD pin). If this flag is set, the slave will only receive AS-i telegrams from IRD pin.

LED output sends MAN2-coded AS-i signals:

- if *master_bit* is set, the converted signal stream is appearing on the AS-i line, or if *master_bit* is cleared and *irlock_bit* is set, the slave responses will appear

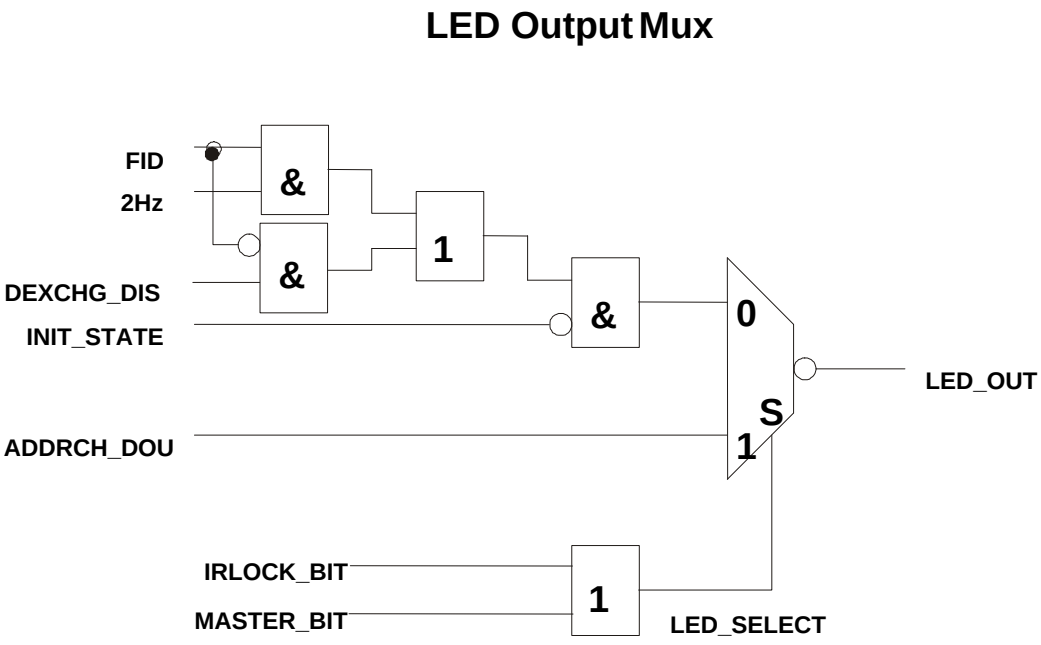


Figure 2: LED Output Control Principle

Under all other conditions the LED output operates as a status indicator. The LED can be on or off, where *LED off* corresponds to *logic high level* at the LED pin (*LED_OUT*). Vice versa *LED on* corresponds to *logic low level* on *LED_OUT*. The LED will display the following status information:

- LED Off:
  - **RESET**: Either DSR pin is static low or the IC is executing its reset/initialization procedure. This procedure takes approximately 2 ms. The initialization procedure will be performed after a power-on reset, a software reset (call RES), or an external reset.
  - **Communication ON:** The slave can respond to DEXG master calls if its *data exchange disable flag* (*DATAEXCHG_DIS*) has been cleared.

    The *DATAEXCHG_DIS* is set during initialization of the A²SI. It will be cleared by the first write parameter request (WPAR) addressing the considered slave.
- LED Constant On:
  - **Communication OFF:** After an IC reset, the *data exchange disable flag* (*DATAEXCHG_DIS*) is set and causes the LED to become constant on. Following scenarios may cause an IC reset:
    - power-on reset, external reset, execution of a software reset (call RES, BR01)
    - reset caused by the integrated watchdog

- an access to a non-implemented EEPROM register

- The LED is also constant on if the IR-addressing channel was selected and no communication takes place. A turned on LED represents the logical high level of the MAN2-coded output signal.

- LED Flashing (2Hz):

  - **Periphery Fault**: In case of a periphery fault (logic high at FID), the LED flashes with a frequency of 2 Hz. Since the FID signal has higher priority than the *Communication OFF* state, the LED will remain flashing even if the Communication is off (*data exchange disable flag* is set).

7.4. IR-Addressing Operation

If the A²SI has detected a valid telegram at the IR-input port (refer to chapter 7.2.7), the IRD pin operates as AS-i telegram input and the LED pin operates as slave response output. Both, the input and the output process MAN-II-coded signals. In both cases, emitted light corresponds to *logic high* in the MAN-II-coded signal. The IR-input automatically adapts to the amplitude of the photo current signal supplied by a photo-diode.

7.5. Data Port Operation

7.5.1. Data Port Configuration

Although the A²SI can still store the AS-i Slave IO-Configuration Code it does not decode the value to configure the direction of the Data-Port signals. The A²SI rather has distinctive Data-Out and Data-In ports which do always work in parallel.

If bi-directional Data I/O is desired on top of a single Data-Port only (for backwards compatibility), the Data-Out pins and the Data-In pins need to be shorted on the circuit board respectively and the non-vololatile *Multiplex* flag has to be set TRUE.

In that case the output ports will switch to high impedance state for a certain time following the rising edge of the Data-Strobe and allow the input data to be put on the Data-Port.

The input data will be read inverted if the non-volatile *Invert_Data_In* flag is TRUE. This feature will simplify the circuitry for NPN-inputs.

Note: The Multiplex and the Invert_Data_In flags are Configuration flags which are stored in the Firmware region of the internal E²PROM. For a complete overview of the E²PROM content please see the A²SI Application Notes.

The parameter port is always in bi-directional mode. The input data is the result of a wired-AND between the open drain output drivers and the application drivers.

7.5.2. A²SI Versus ASI3+ Timing

The timing of data and parameter ports has been changed compared to the ASI3+. The A²SI provides longer strobe pulses. For more information consult the A²SI Data Sheet.

8 Application Info

8.1. Pin Description

Table 4: Pin List

28-Pin SSOP Pin Number	Name	Type	Description	Remarks
1	ASIP	INOUT	TO BE CONNECTED TO THE AS-I-LINE ASI+ VIA REVERSE POLARITY PROTECTION DIODE	
2	ASIN	INOUT	TO BE CONNECTED TO THE AS-I-LINE ASI-	ASIN should be interconnected with the 0V-pin. Route from ASI- to ASIN and then to 0V.
3	0V	SUPPLY	Common 0V for all IC-ports except ASIP/ASIN (usually to be connected to the AS-i-line ASI-)	Must to be interconnected with GND. This interconnection should be as short as possible to avoid voltage drops between the pins.
4	IRD	IN	Addressing channel input	In slave mode connected to a photo-diode, in master/repeater mode regular CMOS-input. Note: In slave mode this is a very sensitive input.
5	FID	IN	Input peripheral fault indication	Refer to DI0
6	OSC2	INOUT	Crystal oscillator (8 MHz x-tal)	The x-tal oscillator does not require additional electronic components.
7	OSC1	IN	Crystal oscillator / external clock input	
8	DO3	OUT	Output of data D3	Open-drain output
9	DO2	OUT	Output of data D2	Open-drain output
10	DO1	OUT	Output of data D1	Open-drain output
11	DO0	OUT	Output of data D0	Open-drain output
12	GND	SUPPLY	Digital IO ground	NOTE: GND and 0V must be connected externally by low resistance and low inductance wiring.
13	P3	I/O	Input/output of parameter P3	Open-drain output, input refer to DI0
14	P2	I/O	Input/output of parameter P2 / Receive Strobe in ”Master Mode”	Open-drain output, input refer to DI0
15	P1	I/O	Input/output of parameter P1 / Power Fail in ”Master Mode”	Open-drain output, input refer to DI0
16	P0	I/O	Input/output of parameter P0 / Data Clock in ”Master Mode”	Open-drain output, input refer to DI0
17	DI0	IN	Input of data D0	Contains an internal pull-up transistor, The input voltage is internally clamped to 5V (consider higher input current if V_{IN} > 5V)
18	DI1	IN	Input of data D1	Refer to DI0

28-Pin SSOP Pin Number	Name	Type	Description	Remarks
19	DI2	IN	Input of data D2	Refer to DI0
20	DI3	IN	Input of date D3	Refer to DI0
21	PST	INOUT	Parameter strobe output	Open-drain output, input refer to DI0 The input is only used for production test
22	DSR	INOUT	Data strobe output/reset input	Open-drain output, input refer to DI0
23	U5RD	SUPPLY (DIG)	Digital 5V supply input	NOTE: U5RD must be interconnected with U5R externally by low resistance and low inductance wiring.
24	LED	OUT	Output LED "AS-i-Diagnosis" / addressing channel output	Open-drain output, there is an input for test reasons
25	CAP	INOUT	RC blocking circuit	Recommended values for R and C depend on the IC version, refer to Table 5
26	U5R	Voltage OUT	Stabilized 5V supply	Can be used to that supply external circuits with up to 4mA
27	U_{OUT}	Voltage OUT	Unstabilized external circuit (e.g. sensor, actuator) supply	approximately V_{UIN} minus 7 volt
28	U_{IN}	SUPPLY	Input of the power supply block	Usually to be connected to the AS-i-line ASI+ via reverse polarity protection diode

8.2. External Components

In order to optimize the input impedance of the IC, the CAP pin needs to be connected to the 0V pin by serial connection of a resistor R_{CAP} and a capacitor C_{CAP}. The capacitor C_{CAP} defines the internal low-pass filter time constant; lower values decrease the impedance but improve (shorten) the turn-on time; higher values do not improve the impedance but do increase turn-on time. Turn-on time also depends on the load capacitor at U_{OUT}. After connecting the slave to the power, the capacitor at UOUT is charged with the maximum current I_{UOUT}. The impedance will increase when the voltage allows the analogue circuitry to fully operate. Table 5 shows recommended values that ensure optimal input impedance on various revisions of the device.

*Table 5: Recommendations for **C_{CAP}** and **R_{CAP}***

Revision Code [1]	Recommended for optimal impedance	Remarks
"Blank" (A)	C_{CAP} = 10 nF, R_{CAP} = 1200 ohms	Initial revision produced until December 2000
B	C_{CAP} = 4.7 nF, R_{CAP} = 430 - 680 ohms	Optimized for high-volume production. Introduced in January 2001
C	C_{CAP} = 4.7 nF, R_{CAP} = 430 - 680 ohms	Improved high-volume revision. For details see A²SI Rev. C Release Notes Introduced in July 2002

1 See also Data Sheet section 11 Package Marking.

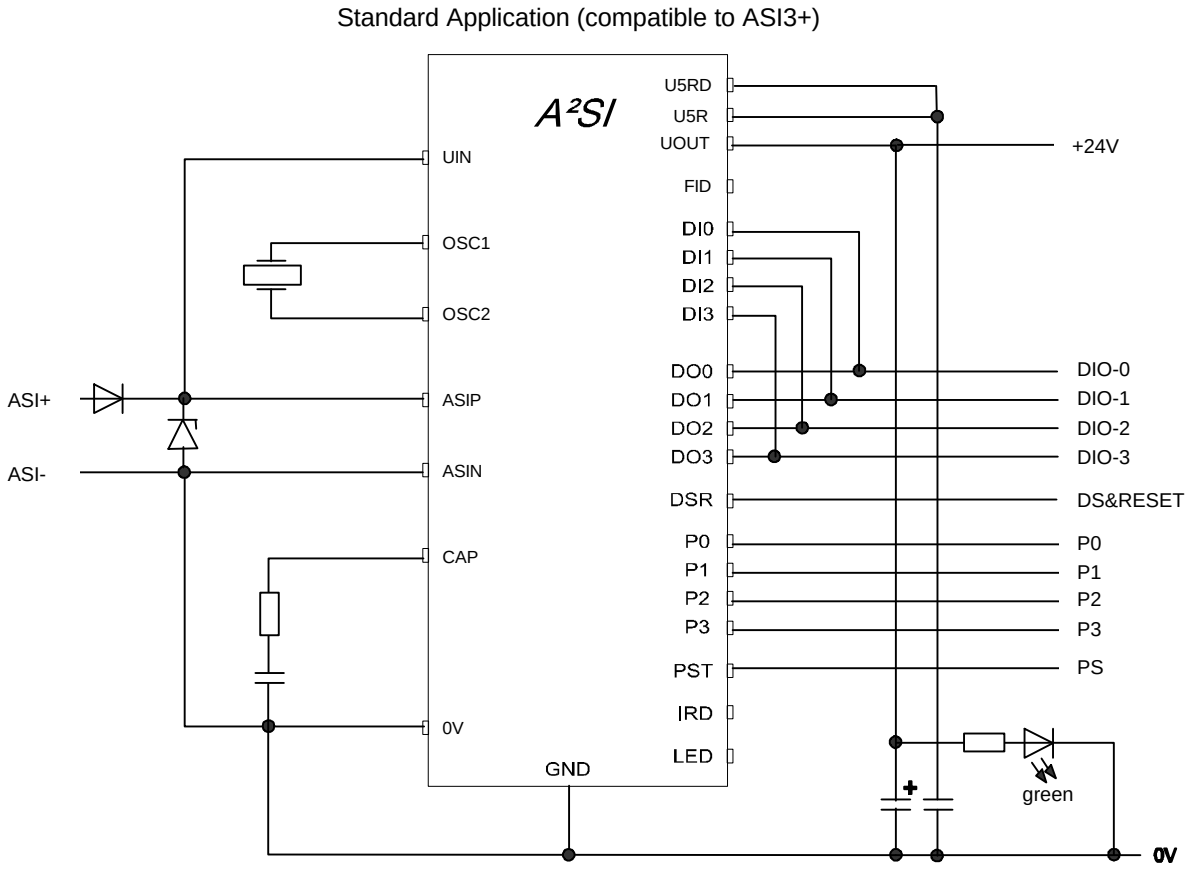
In order to achieve optimal operation of the circuit, few external components are required. Table 6 lists all required external components either concerning a minimum requirement or a more sophisticated solution.

Table 6: A²SI External Components

Pin 1 to pin 2 or Pin to external node	**External components**		**Remarks**
	Minimum requirement	**Optimal solution**	
U5R, U5RD to 0V	1µF electrolyte capacitor in parallel 10 nF ceramic capacitor	2.2µF electrolyte capacitor in parallel 100 nF ceramic capacitor	In order to minimize digital noise at the AS-i line, U5R and U5RD can be interconnected through a resistor. Keep the caps at U5R or split them.
U_{OUT} to 0V	10µF electrolyte capacitor in parallel 100 nF ceramic capacitor	A 100 Ohms resistor in serial to a 10µF electrolyte cap will optimize the settling time of the voltage at U_{OUT}.	Higher value of the electrolyte capacitor is recommended if there are strong load current changes.
OSC1 to OSC2	8.000 MHz standard x-tal, dedicated load capacitance approximately 7 ... 15pF		Calibration tolerance < 60ppm
LED to U_{OUT}		Pull-up resistor typical 100 kohm	If no LED is being connected and if the PCB is causing a high parasitic capacitance at the LED pin
DSR to U5R or U_{OUT}		Pull-up resistor typical 22 kohm	In order to avoid EMC problems (accidental reset of the IC due to strong EMI).
U_{IN} to reverse polarity protection diode or ASI+		10 µH inductor	Avoids RF oscillations on small PCBs.
ASIP to ASIN, 0V, GND If applicable U_{IN} to ASIN, 0V, GND	Suppressor diode 39V, 0.5W		To comply with the AS-i Complete Specification **[1]**, a reverse polarity protection diode must be applied.
IRD to 0V		200 Ohms	Reduces the sensitivity of the IRD input (slave mode) if there are cross-talks on small PCBs.
IRD to U5R		Pull-up resistor typical 5.6 kohm	Ensures in master mode that a open IRD input does not cause a continuously “on” sender stage and subsequently a thermal shut down

8.3. Application Circuits

Following figures show typical application cases of the A²SI IC. In order to demonstrate the backward compatibility of the A²SI, Figure 3 shows an application circuit in which the A²SI is replacing an ASI3+ circuit (for more information about IO-port configuration refer to section 7.5).



Remark: depending on I/O-configuration, DO- and DI-ports are connected and Multiplex-Flag is set

Figure 3: ASI3+ Compatible Standard Application of the A²SI IC

The current through the electronic inductor is limited. If the application requires higher currents, the electronic inductor can be deactivated as illustrated in **Figure 4. Figure 5** shows how the A²SI circuit can be used to perform the analogue digital interface between AS-i-line and the master electronics. This figure shows that the IC can be used in repeater applications as well. Finally, **Figure 6** shows in principle how to build an application circuit that is using the IR-port.

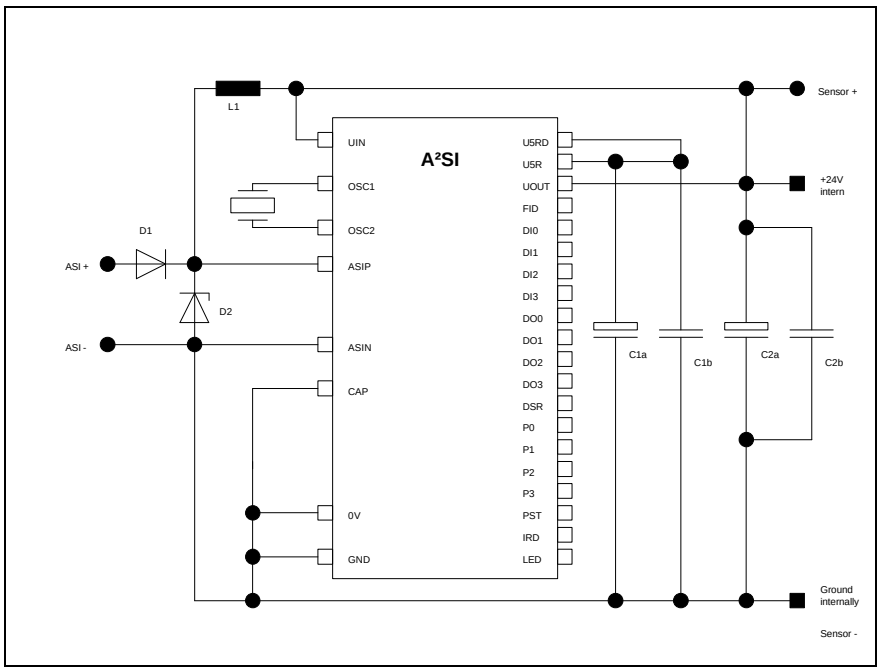


Figure 4: Application Proposal with Deactivated Electronic Inductor

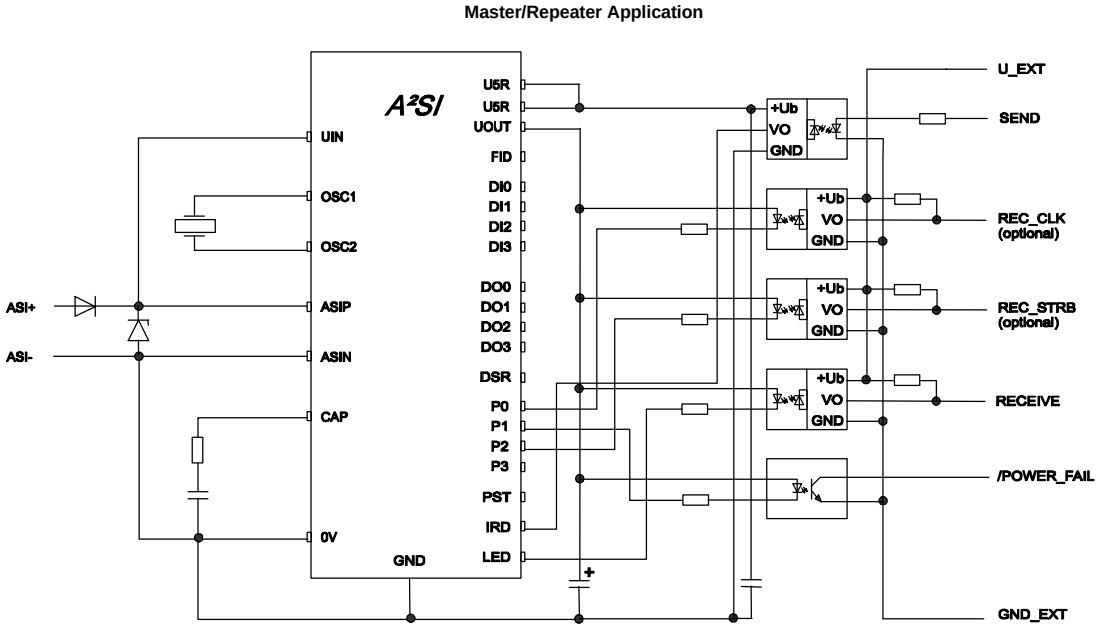


Figure 5 : A²SI Master/Repeater Application Circuit

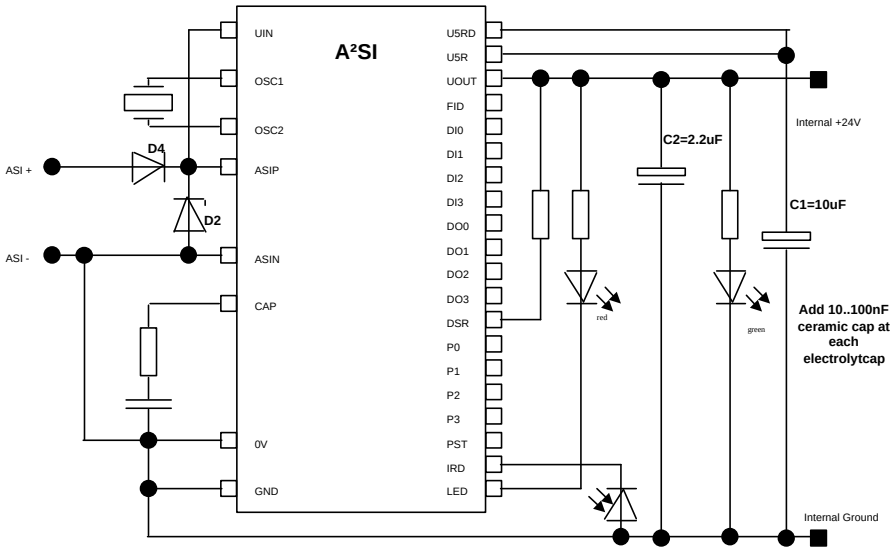


Figure 6: Standard Slave Application Using IR-Addressing Feature

8.4. Critical Parasitic Loads

The function of the A²SI circuit is guaranteed within the operating conditions that are specified in A²SI Data Sheet. if conditions are violated, there might be a risk of malfunctions. The designer of an application circuit, in particular the designer of a PCB layout, can run into difficulties if the influence of parasitic loads is underestimated.

Table 7: Critical Parasitic Loads

Parasitic Load	Malfunction	Reason	Recommendation
Parasitic load capacitance at DSR is too high.	IC performs a reset after performing a DEXG call	DSR is tied to low for more than 35 ms	Implement a pull-up resistor or decrease the pull resistor to U5R (or U_{OUT})
Unused (floating) DSR pin	EMC problems due to accidental resets	Internal pull-up resistor does not keep DSR stable on high.	Implement a pull-up resistor to U5R (or U_{OUT})
Parasitic load capacitance at LED is too high or LED is floating.	IC enters test mode accidentally	IC detects signal transitions at LED while DSR is being low.	Implement a pull-up resistor or decrease the pull resistor to U5R (or U_{OUT})
Overloaded OSC1/OSC2 pins (parasitic caps)	x-tal oscillator does not work	The IC contains a low-power oscillator that is not dedicated to drive external loads	Keep the parasitic cap between OSC1 and OSC2 below 7 pF and keep the parasitic load to ground below 2 pF.

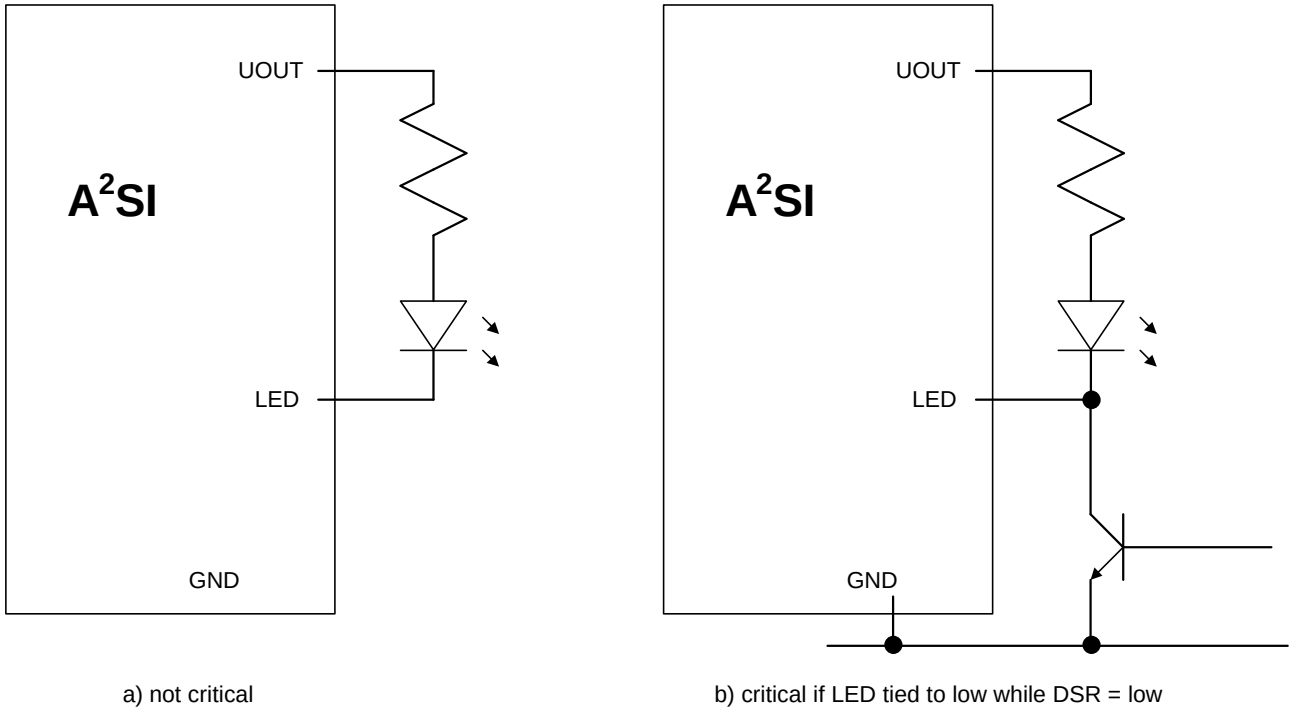
8.5. Test Mode

The A²SI circuit has a built-in test mode that is used for IC testing at ZMD. For this particular purpose the LED pin has an input function as well. Although this input has no relevance for normal A²SI applications, it shall be considered by the designer of the application circuit to prevent incidental entry into test mode. The IC user is not supposed to use this test mode. The test mode functionality can be subject to change without any notice.

Incidental entry into test mode may happen if recommended operating conditions are violated. To prevent activating test mode within an application circuit, following recommendation should be considered:

- LED pin should not toggle while the IC is performing an external reset or in particular should not toggle if DSR is pulled down (logic low).

Parasitic capacitance at the pins LED and DSR should not exceed the maximum values. Otherwise, the IC may detect signal transitions at LED input during power-up. An unused and floating LED pin may cause an unreliable application circuit. To avoid this, connect the LED pin to GND or via an appropriate pull-up resistor to U_{OUT}.



a) not critical

b) critical if LED tied to low while DSR = low

Figure 7 : LED Pin Application Circuits

Figure 7a shows a typical application circuitry for the LED pin. As long as the parasitic capacitance from LED to GND does not exceed the maximum value, the IC will not enter test mode incidentally.

Figure 7b shows a critical application circuit that could cause problems if it is not made sure that the LED will not toggle while DSR is pulled-down.

8.6. PCB Design Recommendations

To assure correct operation of the IC, following facts should be considered when designing a PCB for an A²SI application:

- Interconnection between X-tal and IC should be as short as possible and large parasitic capacities at the pins should be avoided.
- An IR photo-diode between IRD and 0V should be connected with shortest possible wires to avoid interference from parasitic signals.
- Pin 0V and GND must be directly connected. Also, pin U5R and U5RD have to be interconnected with low-ohmic resistance. The de-coupling capacitors between U5R/U5RD and GND/0V shall be placed as close as possible to the U5R and 0V pin, respectively.
- De-coupling capacitors between U_{OUT} and GND/0V shall be placed as close as possible to U_{OUT} and 0V pins, respectively. This recommendation is the same if a resistor is put in series with the electrolyte capacitor.
- The ground node of the external slave electronic circuitry (that is controlled by the A^2SI) should directly be connected to A^2SI GND pin (the wire should **not** pass through to pin 0V and then to pin GND). It should have a low-ohmic resistance and a low inductance.
- The connection of the ASIN pin to the 0V pin should not run via the GND pin. This wiring resistance may have some inductance (maximum value not yet defined). The optimal routing is ASI- to ASIN, then to 0V, and then to GND.
- Parasitic capacitors from the pins LED and DSR to Ground (0V/GND) should not exceed the value mentioned in the A^2SI Data Sheet.

9 Application Support

9.1 AS-International Association

Documentation and promotional materials as well as detailed technical specifications regarding the AS-Interface Bus Standard are available from:

AS-International Association
Contact - Rolf Becker
Zum Taubengarten 52
D-63571 Gelnhausen
PO Box 1103 Zip (63551)
Tel: +49 6051 47 32 12
Fax: +49 6051 4732 82
Email: as-interface@t-online.de
http://www.as-interface.net

Refer to the Association's website here above for contact info on nine local AS-Interface associations which provide local support within Europe, in the US and in Japan.

9.2 ZMD

A²SI/A²SI-E device related application support requests can be addressed to asi@zmd.de.

9.3 ZMD Application Support Partners

ZMD Application Support Partners:

Bihl+Wiedemann
Flosswoerthstrasse 41
D-68199 Mannheim, Germany
Tel.: +49 621 3 3996 0
Fax: +49 621 3 3922 39
Email: mail@bihl-wiedemann.de
http://www.bihl-wiedemann.de

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